IN THE CLAIMS:

Please amend claims 7, 9-12, 14, 16, 19, 21, 33, 34, and 37 as follows:

1-6. (Canceled)

7. (Currently Amended) ~~An~~ The integrated circuit according to claim 12, ~~including a plurality of transistors, a plurality of passive components, and a level of local metal connections formed within a first insulating layer that is deposited on top of the transistors of the integrated circuit, said integrated circuit comprising:~~

~~a first metal terminal constituting a first stage of contact between one active area of the integrated circuit and a first level of interconnection, having a lower surface that contacts the one active area of the integrated circuit, and having an upper surface that contacts a second stage of contact between the one active area of the integrated circuit and the first level of interconnection;~~

~~a second metal terminal vertically connecting one active area of the integrated circuit to a passive component that directly contacts the upper surface of the first insulating layer; and~~

~~a third metal terminal horizontally connecting two separate active areas of the integrated circuit;~~

wherein ~~each of the first, second, and third metal terminals consists of a single layer of metal formed within a cavity passing completely through the thickness of the first insulating layer such that the metal terminal passes completely through the thickness of the first insulating layer, and~~ the second metal terminal has a lower surface that contacts a junction of one of the transistors of the integrated circuit such that the lower surface of the second metal terminal extends over a boundary of the junction of the one transistor.

8. (Canceled)

9. (Currently Amended) The integrated circuit according to claim ~~7~~ 12, wherein the passive components include capacitors.

10. (Currently Amended) The integrated circuit according to claim ~~7~~ 12, wherein the passive components include inductors.

11. (Currently Amended) The integrated circuit according to claim ~~7~~ 12,
wherein the thickness of the first insulating layer is greater than 0.3 micrometers,
the upper surface of the first insulating layer is plane, and
the first, second, and third metal terminals are made of tungsten.

12. (Currently Amended) ~~The~~ An integrated circuit ~~according to claim 7, further~~ including a plurality of transistors, a plurality of passive components, and a level of local metal connections formed within a first insulating layer that is deposited on top of the transistors of the integrated circuit, said integrated circuit comprising:

a first metal terminal constituting a first stage of contact between one active area of the integrated circuit and a first level of interconnection, having a lower surface that contacts the one active area of the integrated circuit, and having an upper surface that contacts a second stage of contact between the one active area of the integrated circuit and the first level of interconnection;

a second metal terminal vertically connecting one active area of the integrated circuit to a passive component that directly contacts the upper surface of the first insulating layer;

a third metal terminal horizontally connecting two separate active areas of the integrated circuit; and

a second insulating layer above the first insulating layer, the passive component ~~resting on the first insulating layer~~ being set into a cavity formed throughout the thickness of the second insulating layer,

wherein each of the first, second, and third metal terminals consists of a single layer of metal formed within a cavity passing completely through the thickness of the first insulating layer such that the metal terminal passes completely through the thickness of the first insulating layer.

13. (Original) The integrated circuit according to claim 12, wherein the thickness of the second insulating layer is greater than 2 micrometers.

14. (Currently Amended) An integrated circuit comprising:

an onboard memory plane of DRAM cells in a matrix, each of the cells including a control transistor and a storage capacitor;

a plurality of MOS transistors;

a first level of interconnection above the storage capacitors;

a first insulating layer separating the MOS transistors and the base of the storage capacitors; and

a level of local connections including three metal terminals each opening onto each side of the first insulating layer, each of the three metal terminals consisting of a single layer of metal formed within a cavity passing completely through the thickness of the first insulating layer such that the metal terminal passes completely through the thickness of the first insulating layer,

wherein the first metal terminal forms a first stage of contact between one active area of the integrated circuit and the first level of interconnection, has an upper surface that contacts a second stage of contact between the one active area of the integrated circuit and the first level of interconnection, and extends from the one active area of the integrated circuit to the second stage of contact,

the second metal terminal vertically connects one active area of the integrated circuit with one plate of one of the storage capacitors, a lower surface of the one plate of the one storage capacitor extending over at least one boundary of an upper surface of the second metal terminal so that a portion of the lower surface of the one plate rests on the upper surface of the second metal terminal and the remainder of the lower surface of the one plate rests on the upper surface of the first insulating layer, ~~and~~

the third metal terminal horizontally connects two separate active areas of the integrated circuit, and

the integrated circuit further comprises:

a second insulating layer above the first insulating layer; and

a cavity passing through the entire thickness of the second insulating layer, the one storage capacitor being set into the cavity.

15. (Previously Presented) The integrated circuit according to claim 14, wherein the second metal terminal has a lower surface that contacts a junction of the one active area such that the lower surface of the second metal terminal extends over a boundary of the junction of the one active area.

16. (Currently Amended) The integrated circuit according to claim 14, ~~further comprising:~~

~~a second insulating layer above the first insulating layer; and~~

~~a cavity passing through the entire thickness of the second insulating layer and opening onto the upper surface of the second metal terminal;~~

wherein the one plate of the one storage capacitor carpets the bottom and the inside flanks of the cavity.

17. (Previously Presented) The integrated circuit according to claim 16, further comprising:

a third insulating layer above the second insulating layer; and

a contact opening passing through the second insulating layer and the third insulating layer and opening onto the upper surface of the first metal terminal.

18. (Previously Presented) The integrated circuit according to claim 14, wherein the first, second, and third metal terminals are made of tungsten.

19. (Currently Amended) An information processing system including at least one integrated circuit, the integrated circuit comprising:

an onboard memory plane of DRAM cells in a matrix, each of the cells including a control transistor and a storage capacitor;

a plurality of MOS transistors;

a first level of interconnection above the storage capacitors;

a first insulating layer separating the MOS transistors and the base of the storage capacitors; and

a level of local connections including three metal terminals each opening onto each side of the first insulating layer, each of the three metal terminals consisting of a single layer of metal formed within a cavity passing completely through the thickness of the first insulating layer such that the metal terminal passes completely through the thickness of the first insulating layer,

wherein the first metal terminal forms a first stage of contact between one active area of the integrated circuit and the first level of interconnection, has an upper surface that contacts a second stage of contact between the one active area of the integrated circuit and the first level of interconnection, and extends from the one active area of the integrated circuit to the second stage of contact,

the second metal terminal vertically connects one active area of the integrated circuit with one plate of one of the storage capacitors, a lower surface of the one plate of the one storage capacitor extending over at least one boundary of an upper surface of the second metal terminal so that a portion of the lower surface of the one plate rests on the upper surface of the second metal terminal and the remainder of the lower surface of the one plate rests on the upper surface of the first insulating layer, and

the third metal terminal horizontally connects two separate active areas of the integrated circuit, and

the integrated circuit further comprises:

a second insulating layer above the first insulating layer; and

a cavity passing through the entire thickness of the second insulating layer, the one storage capacitor being set into the cavity.

20. (Previously Presented) The information processing system according to claim 19, wherein the second metal terminal has a lower surface that contacts a junction of the one active area such that the lower surface of the second metal terminal extends over a boundary of the junction of the one active area.

21. (Currently Amended) The information processing system according to claim 19, ~~wherein the integrated circuit further comprises:~~

~~a second insulating layer above the first insulating layer; and~~

~~a cavity passing through the entire thickness of the second insulating layer and opening onto the upper surface of the second metal terminal;~~

wherein the one plate of the one storage capacitor carpets the bottom and the inside flanks of the cavity.

22. (Previously Presented) The information processing system according to claim 21, wherein the integrated circuit further comprises:

a third insulating layer above the second insulating layer; and

a contact opening passing through the second insulating layer and the third insulating layer and opening onto the upper surface of the first metal terminal.

23. (Previously Presented) The information processing system according to claim 19, wherein the first, second, and third metal terminals are made of tungsten.

24-32. (Canceled)

33. (Currently Amended) The integrated circuit according to claim ~~7~~ 12, wherein the first insulating layer is a single layer and the only insulating layer provided between the transistors and a base of the passive component.

34. (Currently Amended) The integrated circuit according to claim ~~7~~ 12, wherein the third metal terminal is a local horizontal interconnection that directly connects two separate active areas of the integrated circuit.

35-36. (Canceled)

37. (Currently Amended) The integrated circuit according to claim ~~7~~ 12, wherein the second metal terminal has an upper surface that contacts a base of the passive component, and a lower surface of the base of the passive component extends over at least one boundary of the upper surface of the second metal terminal so that a portion of the lower surface of the base of the passive component rests on the upper surface of the second metal terminal and the remainder of the lower surface of the base of the passive component rests on an upper surface of the first insulating layer.

38. (Canceled)